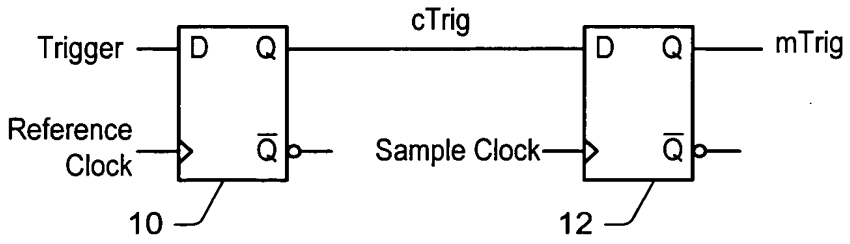


FIG. 1 (Prior Art)

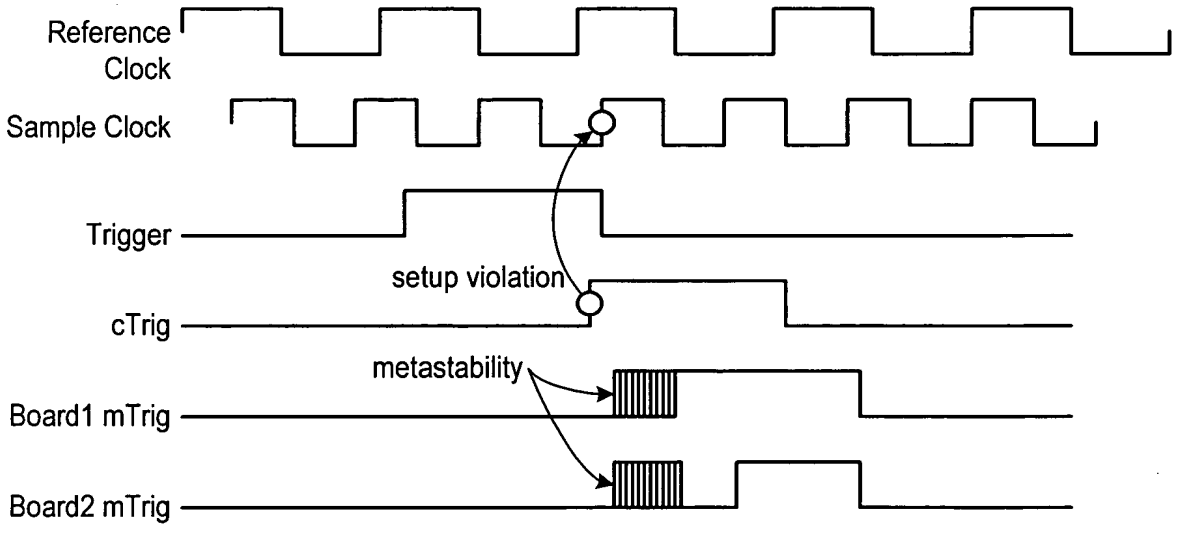
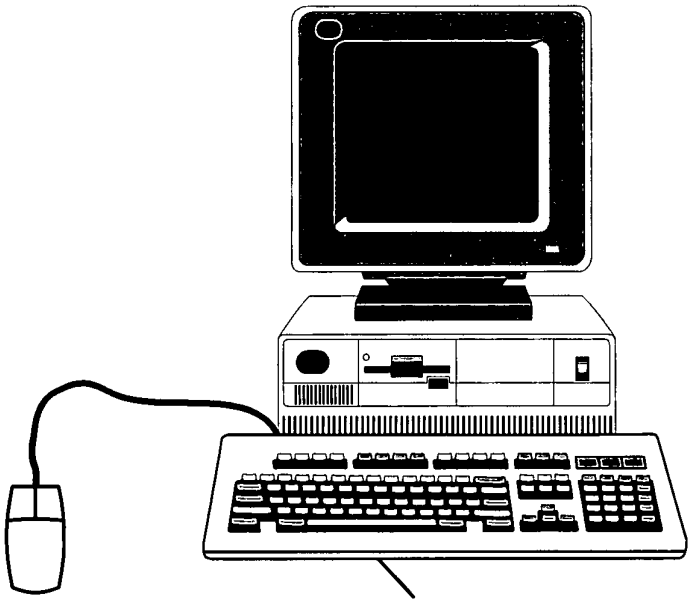


FIG. 2 (Prior Art)



Computer System
82

Figure 3A

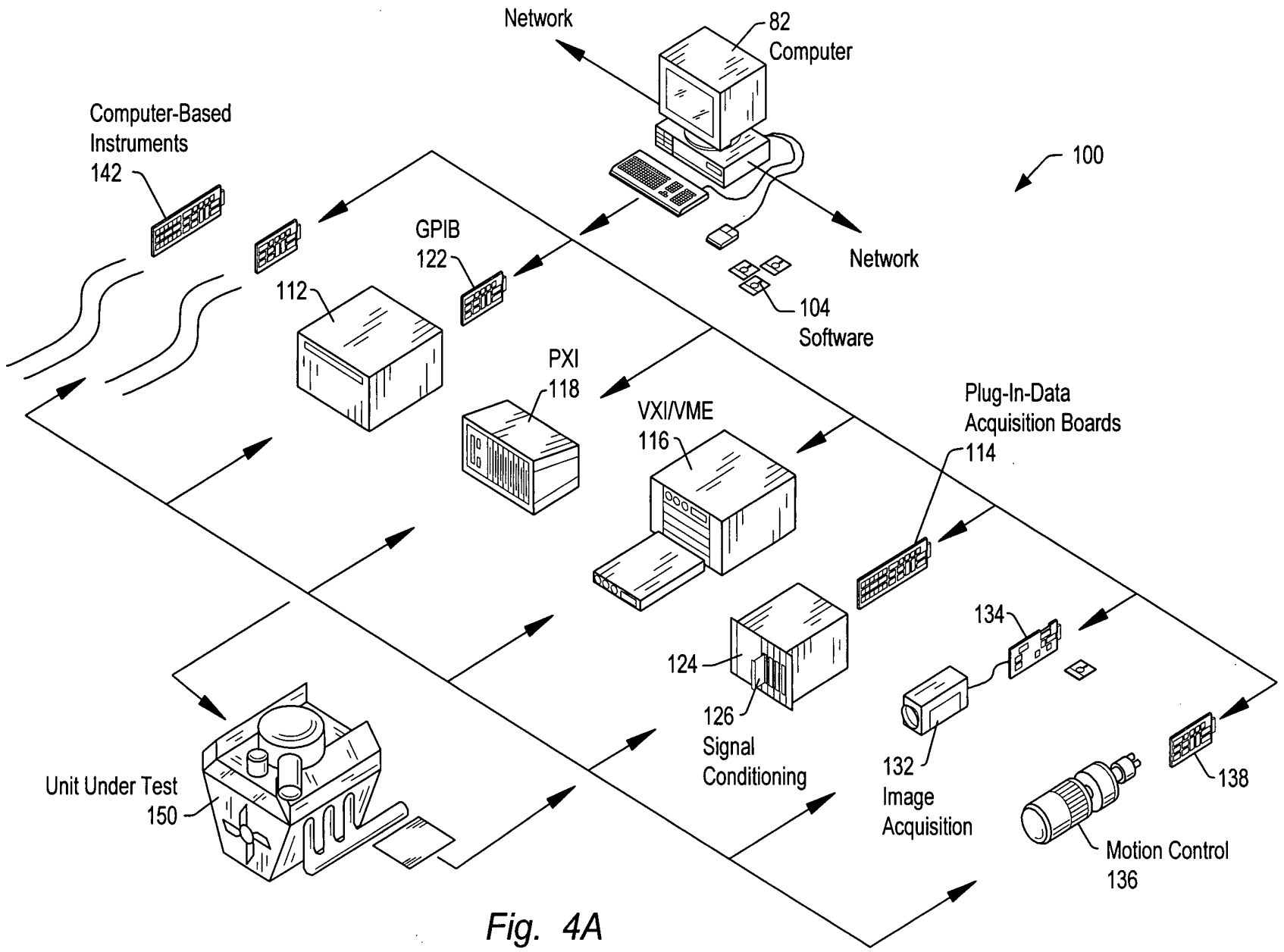

Network
82
Computer
Computer-Based
Instruments
142
100
GPIB
122
112
Network
104
Software
PXI
118
VXI/VME
116
Plug-In-Data
Acquisition Boards
114
134
124
126
Signal
Conditioning
132
Image
Acquisition
138
Motion Control
136
Unit Under Test
150

Fig. 4A

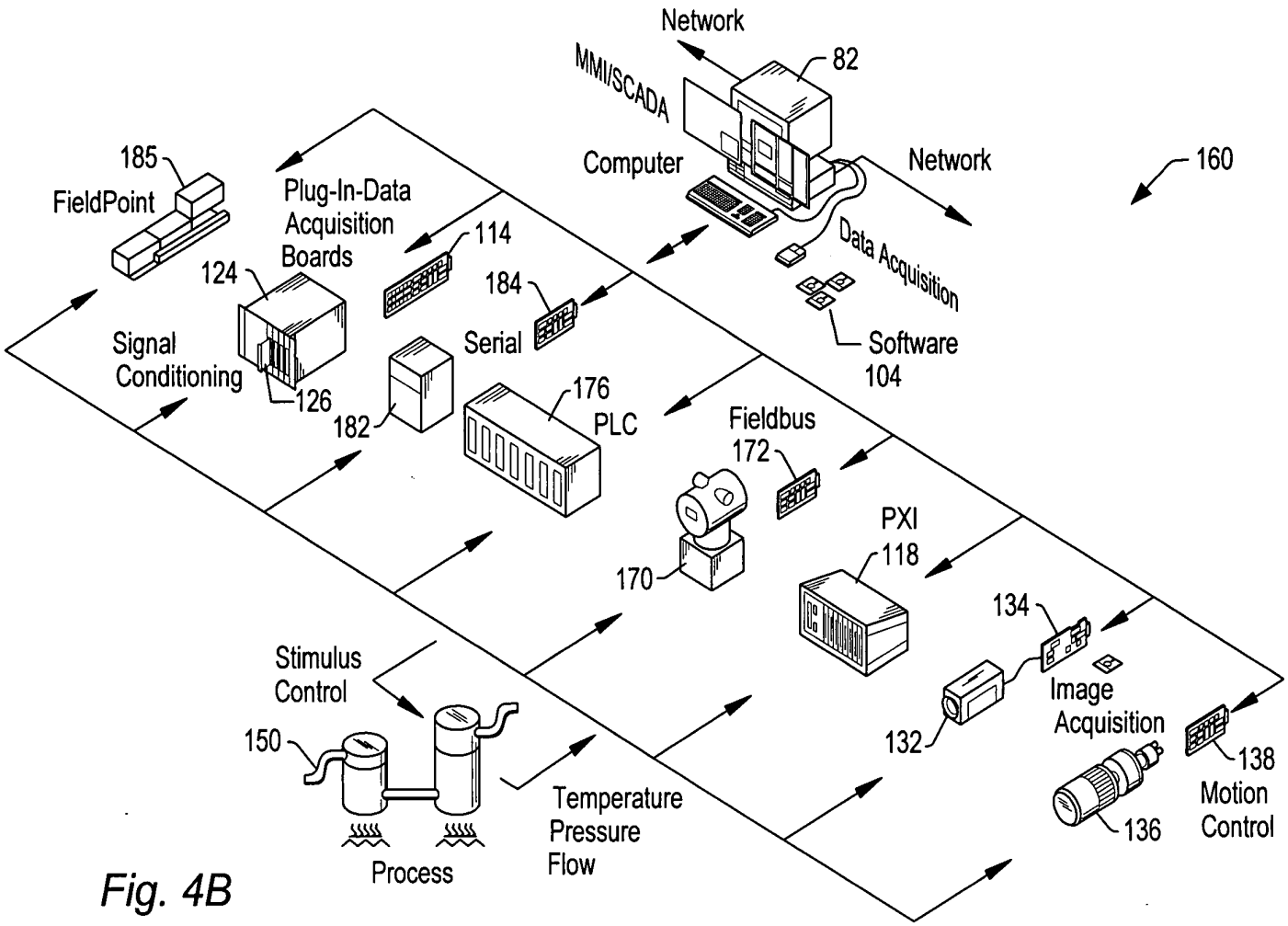

Network
MMI/SCADA
82
Computer
Network
160
185
FieldPoint
Plug-In-Data
Acquisition
Boards
114
124
184
Data Acquisition
Signal
Conditioning
Serial
Software
104
126
182
176
PLC
Fieldbus
172
PXI
118
170
134
Stimulus
Control
Image
Acquisition
150
132
138
Motion
Control
Temperature
Pressure
Flow
136
Process

Fig. 4B

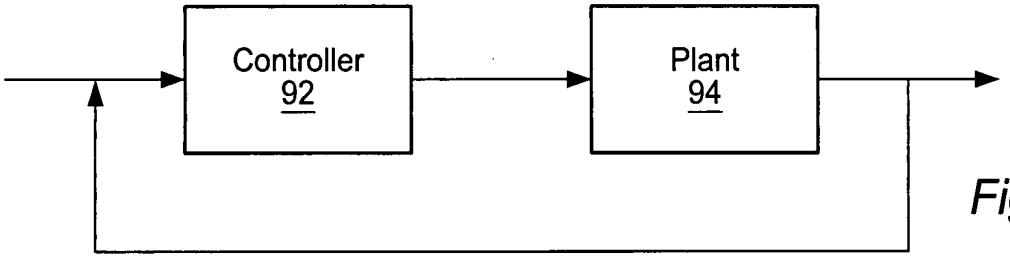


Figure 5A

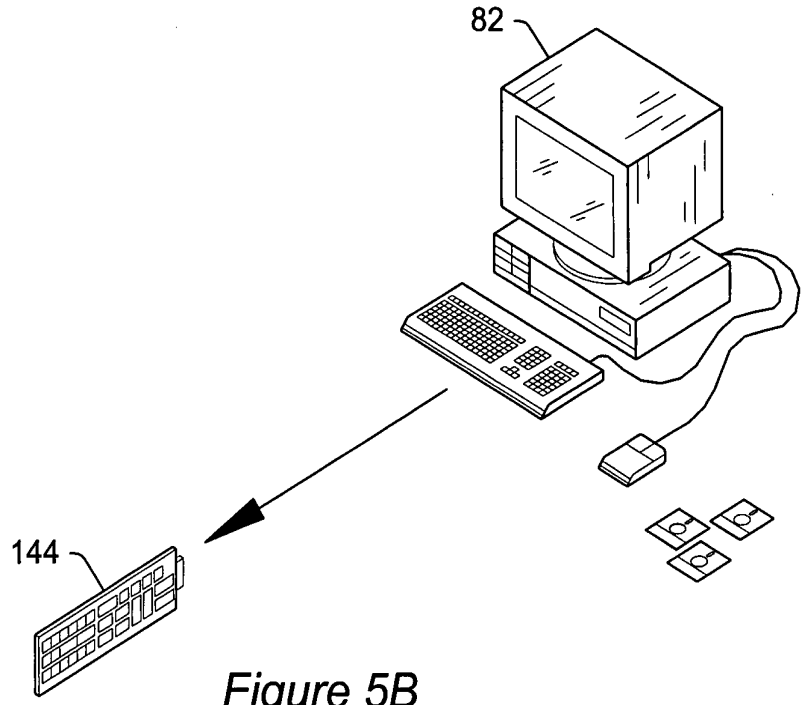


Figure 5B

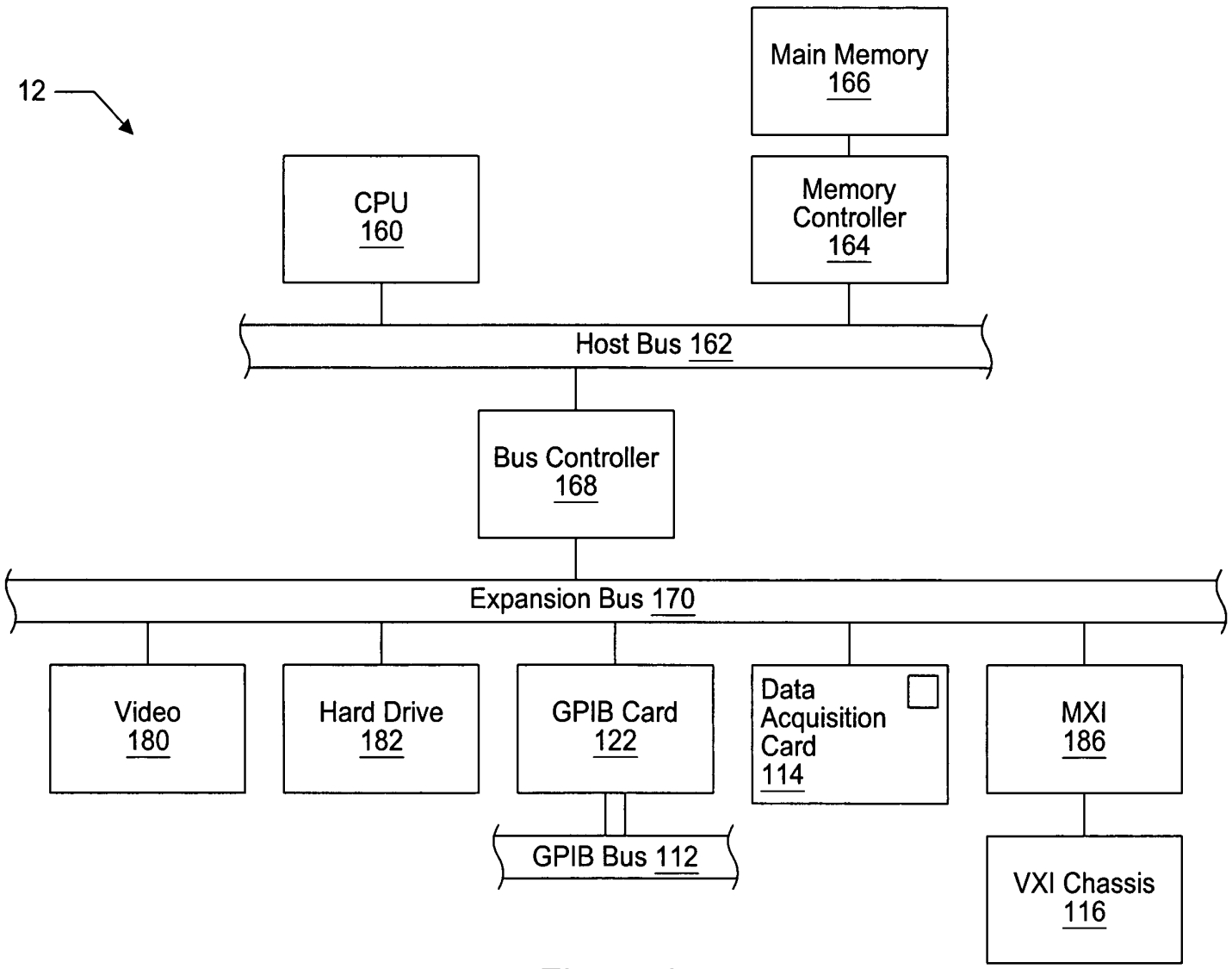

12
Main Memory
166
CPU
160
Memory
Controller
164
Host Bus 162
Bus Controller
168
Expansion Bus 170
Video
180
Hard Drive
182
GPIB Card
122
Data
Acquisition
Card
114
MXI
186
GPIB Bus 112
VXI Chassis
116

Figure 6

Scenarios	Functions							Attributes								
	ConfigureForHomogeneousTrigge	Synchronize	Initiate	IsDone	WaitUntilDone	GetErrorString	GetExtendedErrorInfo	START_TRIG_MASTER_SESSION	REF_TRIG_ORIGINAL_SESSION	SCRIPT_TRIG_MASTER_SESSION	PAUSE_TRIG_MASTER_SESSION	REF_TRIG_IS_FROM_NON_REF_TRIG	TCLK_SYNC_PULSE_SRC	TCLK_SYNC_PULSE_OUTPUT_TERM	TCLK_MIN_PERIOD	SAMP_CLK_DELAY
Single Chassis, Homogeneous Triggers	√	√	√	√	√	√	√									s
Single Chassis, Heterogeneous Triggers		√	√	√	√	√	√	t	t	t	t	t				s
Multiple Chassis		√	√	√	√	√	√	t	t	t	t	t	√	√	√	s

√: all cases
s: sample clock delay is optional in all cases
t: use attributes that pertain to triggers being synchronized

Figure 7

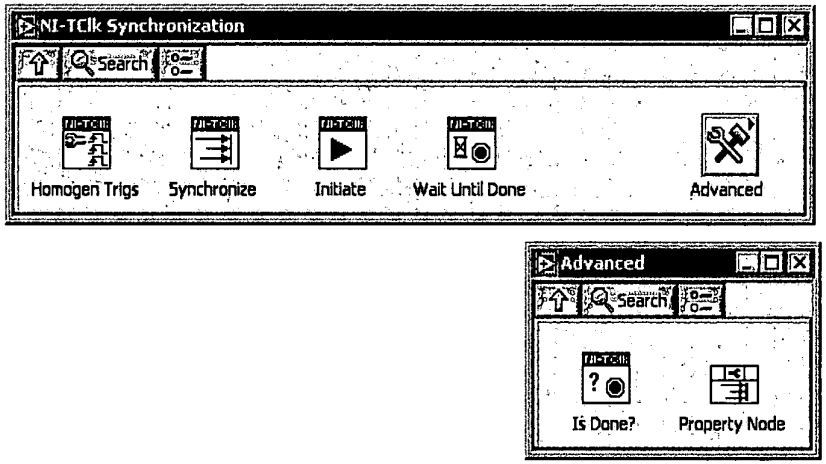

NI-TClk Synchronization
Search
Homogen Trigs
Synchronize
Initiate
Wait Until Done
Advanced
Advanced
Search
Is Done?
Property Node

Figure 8

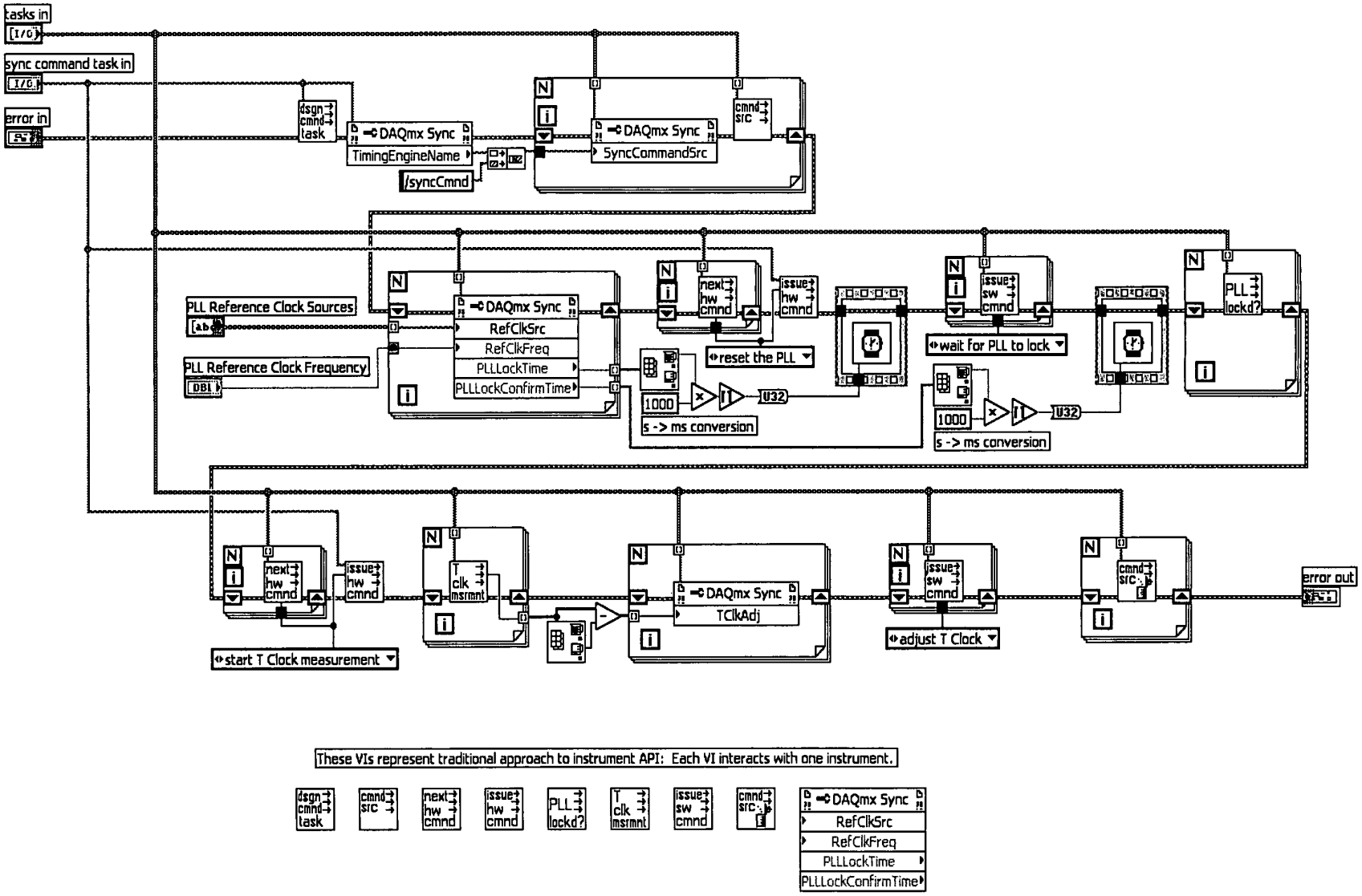

tasks in
I/O
sync command task in
I/O
error in
dsgn cmnd task
DAQmx Sync
TimingEngineName
/syncCmnd
DAQmx Sync
SyncCommandSrc
cmnd src
PLL Reference Clock Sources
PLL Reference Clock Frequency
DBL
DAQmx Sync
RefClkSrc
RefClkFreq
PLLLockTime
PLLLockConfirmTime
next hw cmnd
issue hw cmnd
reset the PLL
1000
U32
s -> ms conversion
issue sw cmnd
wait for PLL to lock
1000
U32
s -> ms conversion
PLL lockd?
next hw cmnd
issue hw cmnd
start T Clock measurement
T clk msrmnt
DAQmx Sync
TClkAdj
issue sw cmnd
adjust T Clock
cmnd src
error out
These VIs represent traditional approach to instrument API: Each VI interacts with one instrument.
dsgn cmnd task
cmnd src
next hw cmnd
issue hw cmnd
PLL lockd?
T clk msrmnt
issue sw cmnd
cmnd src
DAQmx Sync
RefClkSrc
RefClkFreq
PLLLockTime
PLLLockConfirmTime

Figure 9A

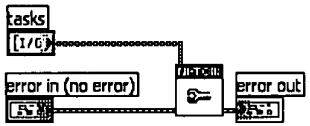


Figure 9B

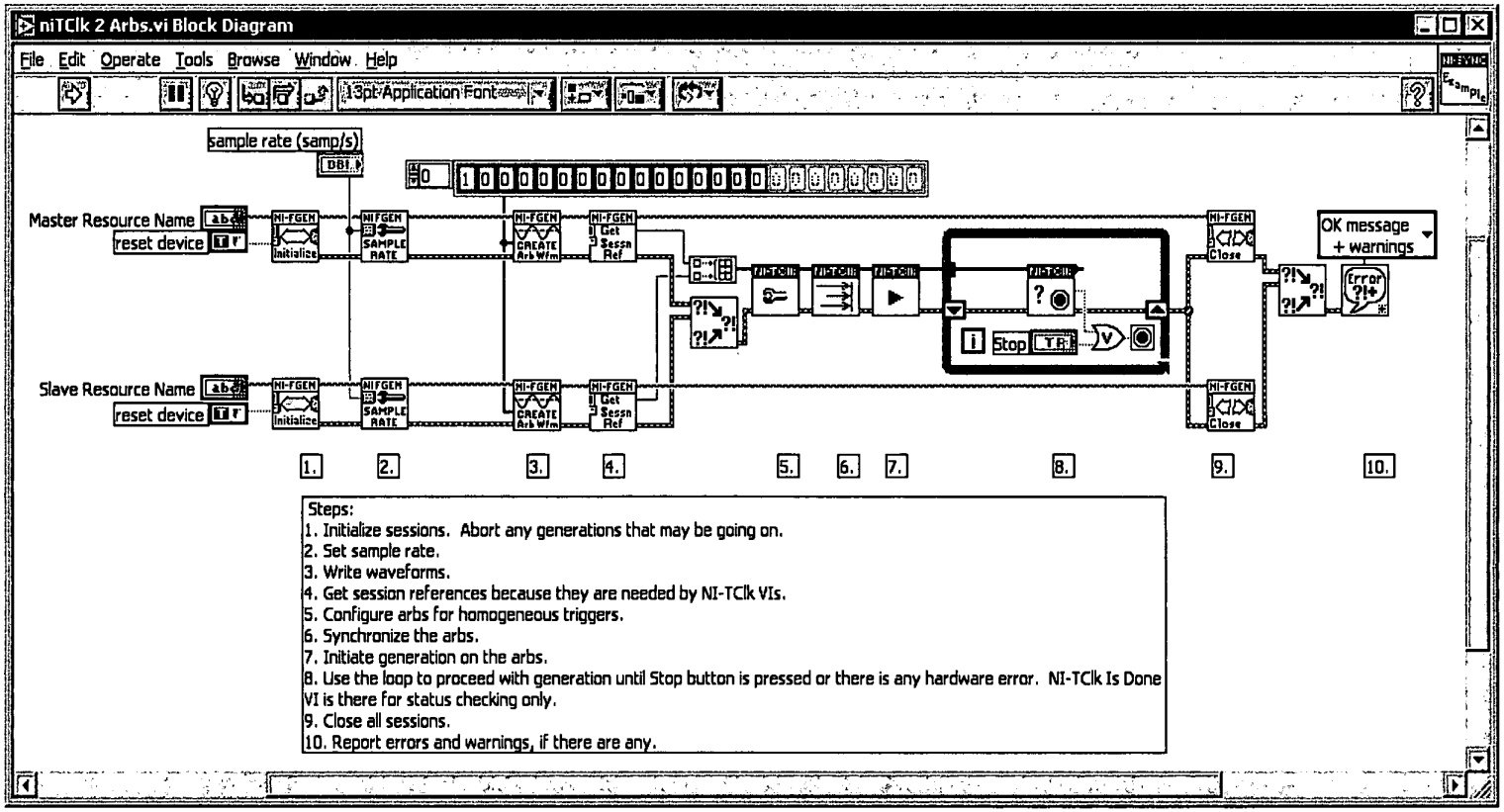

niTClk 2 Arbs.vi Block Diagram
File Edit Operate Tools Browse Window Help
13pt Application Font
sample rate (samp/s)
Master Resource Name
reset device
Slave Resource Name
reset device
Initialize
SAMPLE RATE
CREATE Arb Wfm
Get Sessn Ref
Stop
Close
OK message + warnings
Error
1.
2.
3.
4.
5.
6.
7.
8.
9.
10.
Steps:
1. Initialize sessions. Abort any generations that may be going on.
2. Set sample rate.
3. Write waveforms.
4. Get session references because they are needed by NI-TClk VIs.
5. Configure arbs for homogeneous triggers.
6. Synchronize the arbs.
7. Initiate generation on the arbs.
8. Use the loop to proceed with generation until Stop button is pressed or there is any hardware error. NI-TClk Is Done VI is there for status checking only.
9. Close all sessions.
10. Report errors and warnings, if there are any.

Figure 10

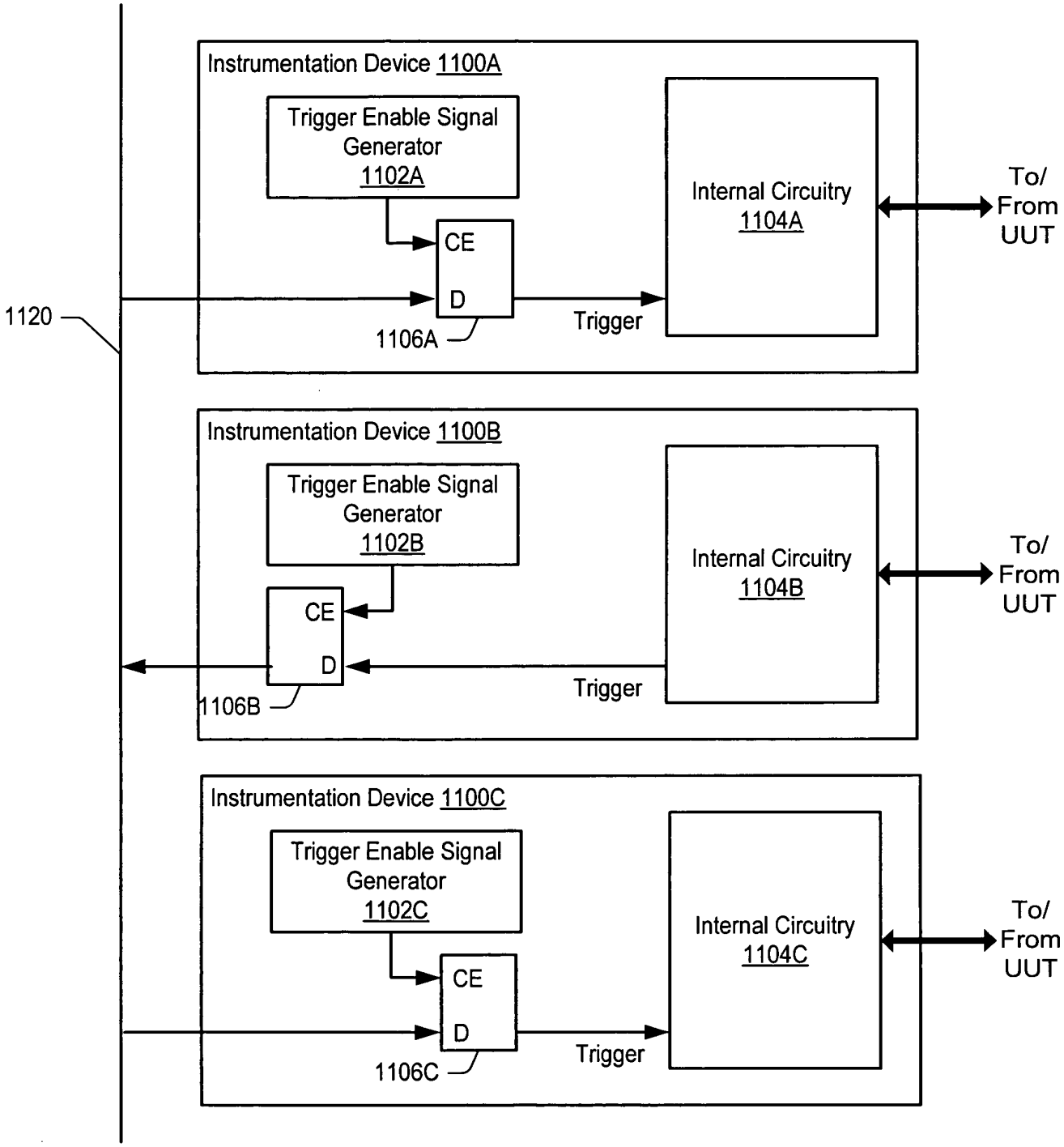

Instrumentation Device 1100A
Trigger Enable Signal Generator 1102A
CE
D
1106A
Trigger
Internal Circuitry 1104A
To/ From UUT
1120
Instrumentation Device 1100B
Trigger Enable Signal Generator 1102B
CE
D
1106B
Trigger
Internal Circuitry 1104B
To/ From UUT
Instrumentation Device 1100C
Trigger Enable Signal Generator 1102C
CE
D
1106C
Trigger
Internal Circuitry 1104C
To/ From UUT

FIG. 11

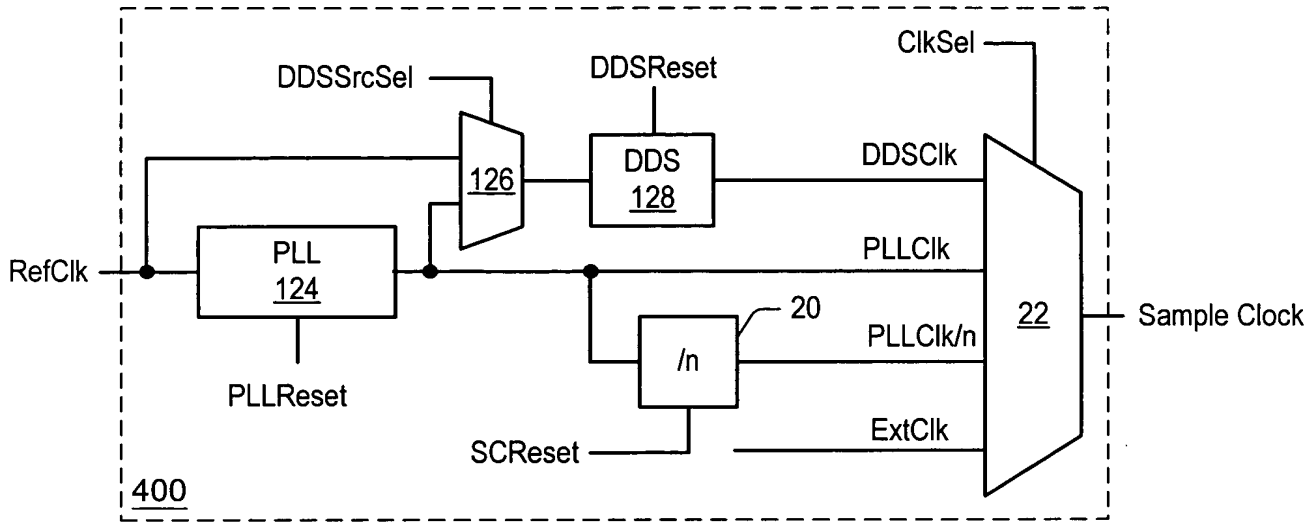

ClkSel
DDSSrcSel
DDSReset
126
DDS
128
DDSClk
RefClk
PLL
124
PLLClk
20
22
Sample Clock
/n
PLLClk/n
PLLReset
SCReset
ExtClk
400

FIG. 12

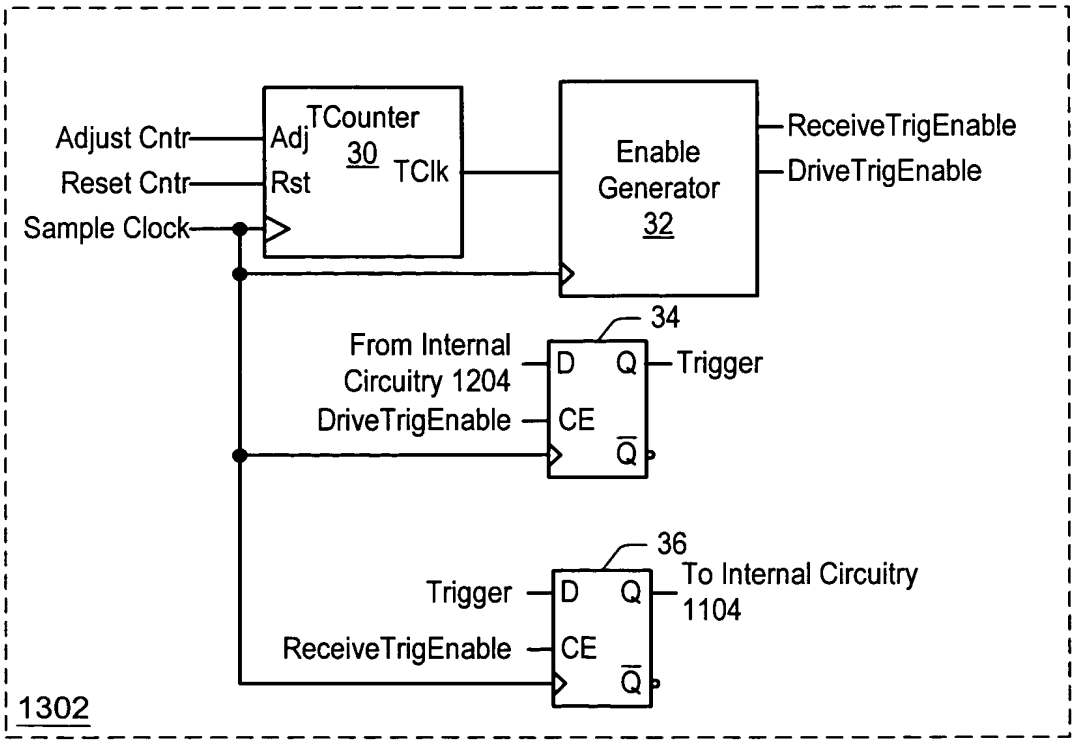

Adjust Cntr
Adj
TCounter
30
Reset Cntr
Rst
TClk
Sample Clock
Enable
Generator
32
ReceiveTrigEnable
DriveTrigEnable
34
From Internal
Circuitry 1204
D
Q
Trigger
DriveTrigEnable
CE
Q
36
Trigger
D
Q
To Internal Circuitry
1104
ReceiveTrigEnable
CE
Q
1302

FIG. 13

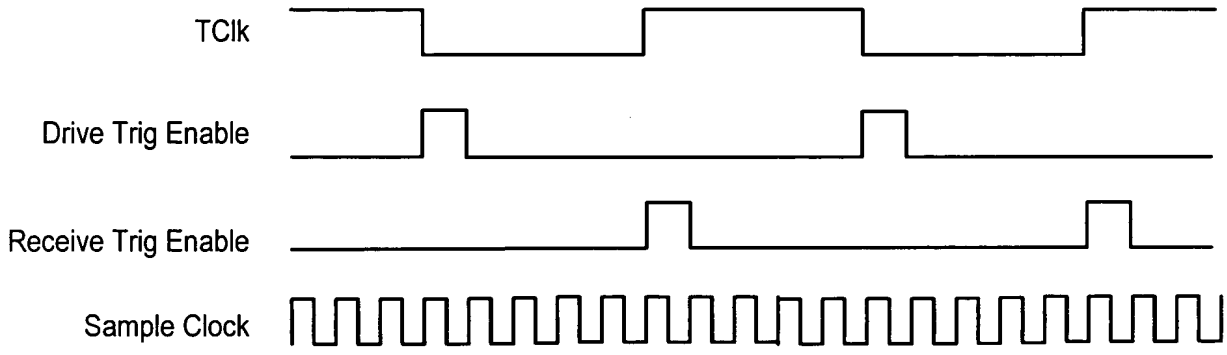


FIG. 14

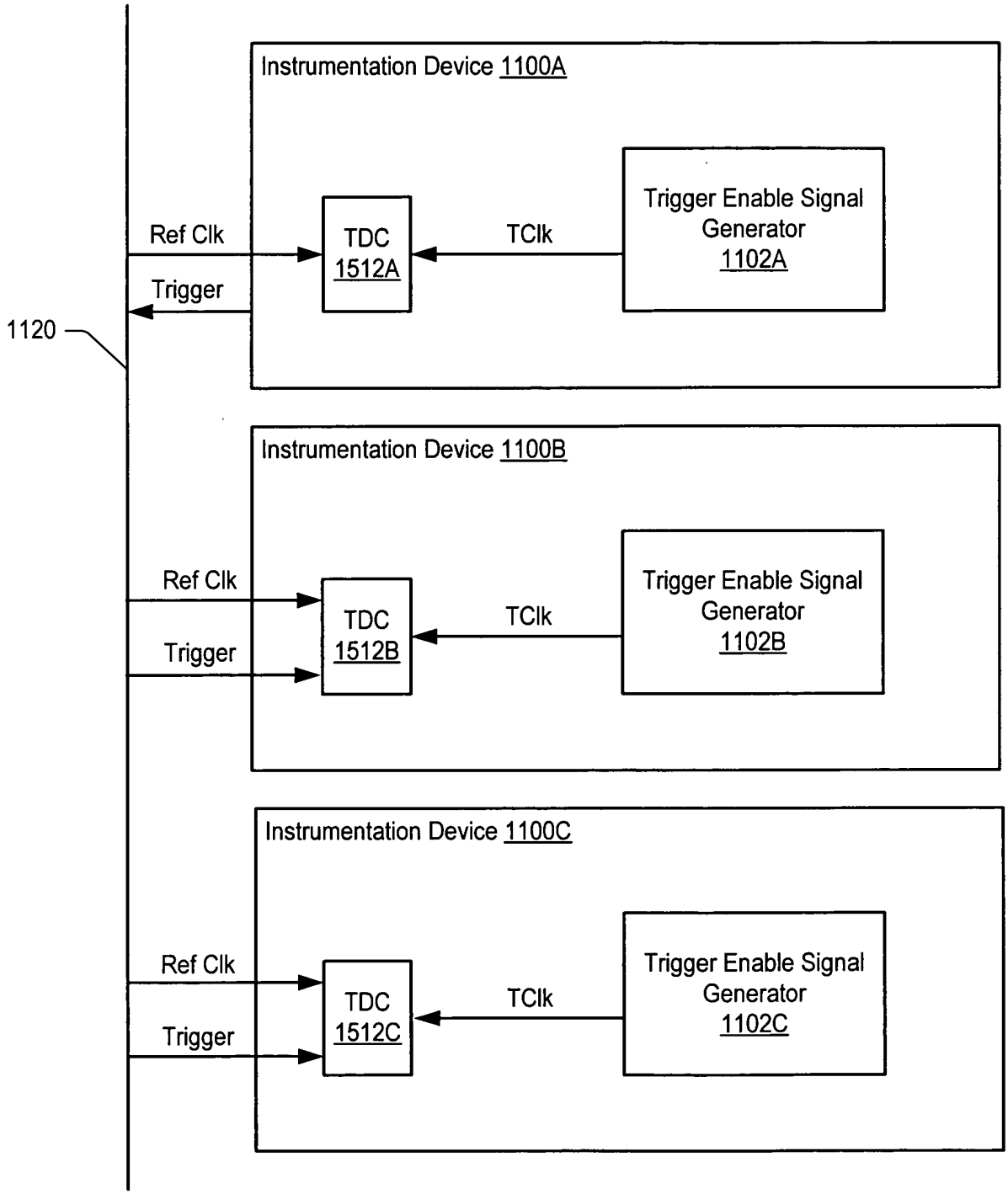

Instrumentation Device 1100A
Trigger Enable Signal Generator 1102A
TDC 1512A
TClk
Ref Clk
Trigger
1120
Instrumentation Device 1100B
Trigger Enable Signal Generator 1102B
TDC 1512B
TClk
Ref Clk
Trigger
Instrumentation Device 1100C
Trigger Enable Signal Generator 1102C
TDC 1512C
TClk
Ref Clk
Trigger

FIG. 15

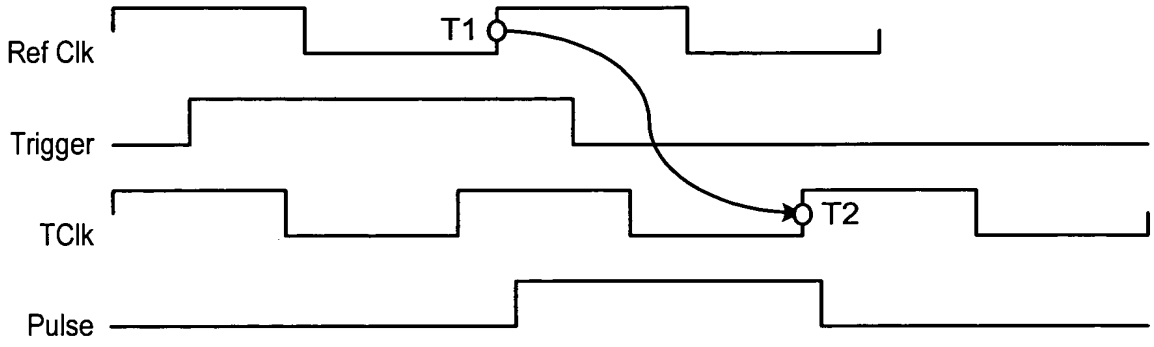


FIG. 16

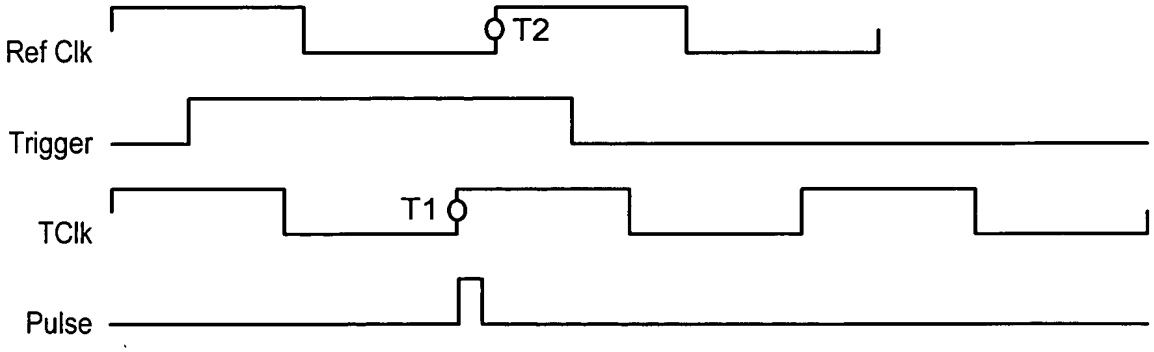


FIG. 16A

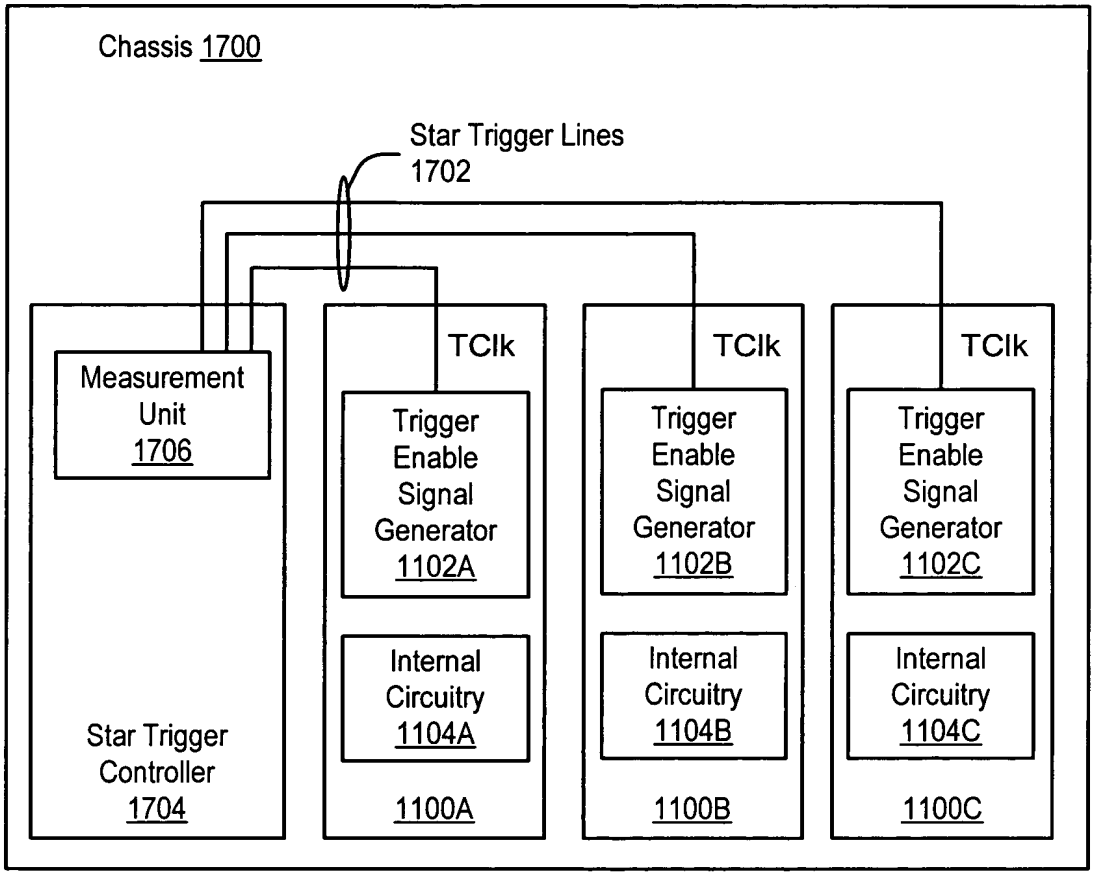

Chassis 1700
Star Trigger Lines
1702
Measurement
Unit
1706
Star Trigger
Controller
1704
TClk
Trigger
Enable
Signal
Generator
1102A
Internal
Circuitry
1104A
1100A
TClk
Trigger
Enable
Signal
Generator
1102B
Internal
Circuitry
1104B
1100B
TClk
Trigger
Enable
Signal
Generator
1102C
Internal
Circuitry
1104C
1100C

FIG. 17

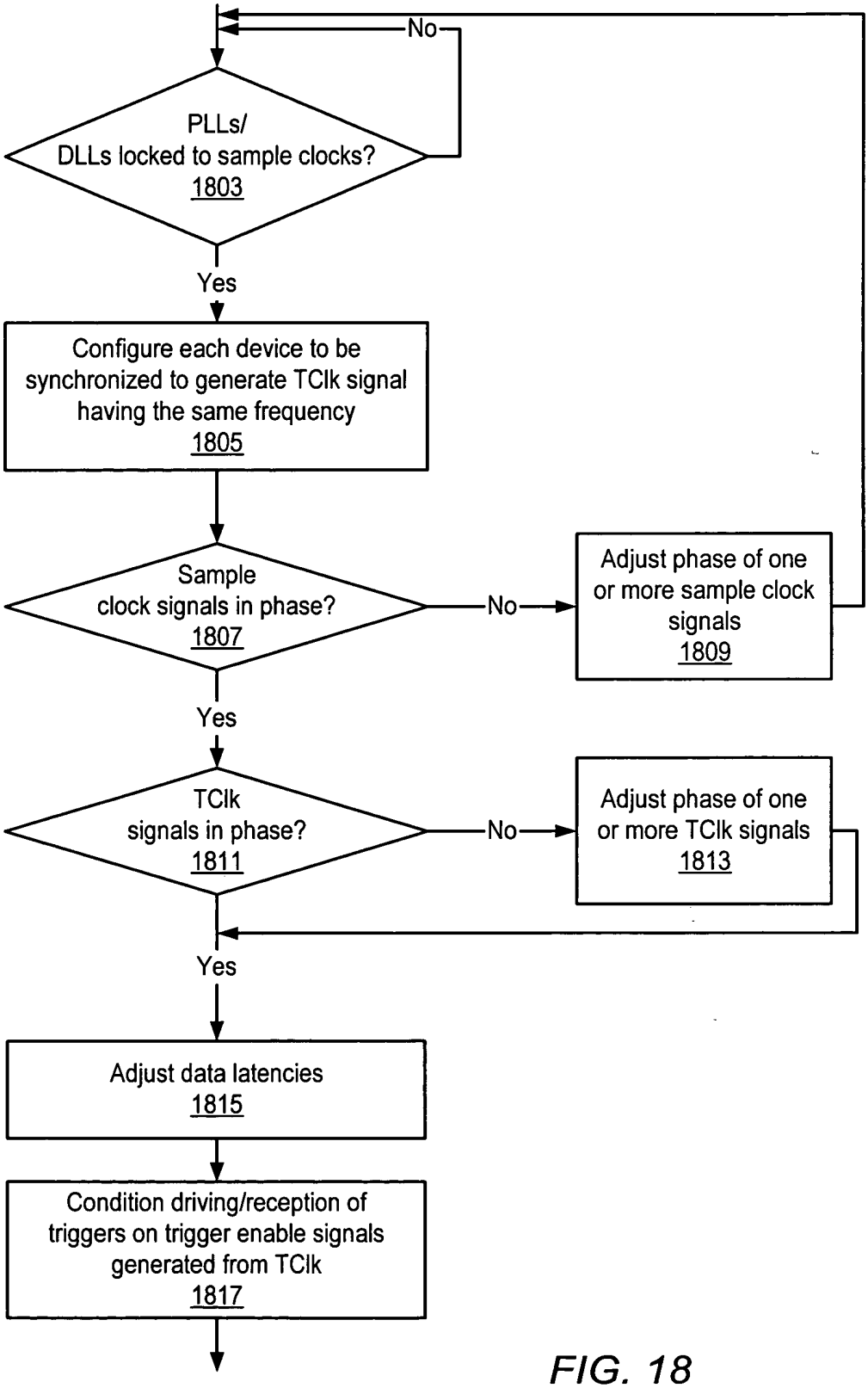

No
PLLs/
DLLs locked to sample clocks?
1803
Yes
Configure each device to be synchronized to generate TClk signal having the same frequency
1805
Sample
clock signals in phase?
1807
No
Adjust phase of one or more sample clock signals
1809
Yes
TClk
signals in phase?
1811
No
Adjust phase of one or more TClk signals
1813
Yes
Adjust data latencies
1815
Condition driving/reception of triggers on trigger enable signals generated from TClk
1817

FIG. 18